

HALO-02-005

January 14, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
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Subject: | Serial No. 10/699,331 10/31/03 |
Ki-Tae Park et al.
A METHOD OF SENSE AND PROGRAM VERIFY
WITHOUT A REFERENCE CELL FOR NON-
VOLATILE SEMICONDUCTOR MEMORY
| _____ |

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

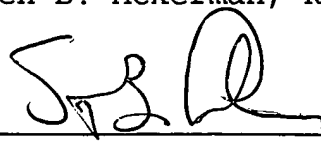
The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on January 27, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 1/27/04

U.S. Patent 6,618,297 to Manea, "Method of Establishing Reference Levels for Sensing Multilevel Memory Cell States," discusses the establishment of boundary current levels directed to providing more than two memory states for a non-volatile memory.

U.S. Patent 6,044,019 to Cernea et al., "Non-Volatile Memory with Improved Sensing and Method Therefor," discusses cancelling inherent noise fluctuations by averaging the sensing of current from a reference cell over a predetermined period of time, thus increasing the accuracy of sensing.

U.S. Patent 5,712,815 to Bill et al., "Multiple Bits Per-cell Flash EEPROM Capable of Concurrently Programming and Verifying Memory Cells and Reference Cells," discusses an improved programming structure in a non-volatile memory array containing multiple bits per cell.

U.S. Patent 5,124,945 to Schreck, "Method and Apparatus for Verifying the State of a Plurality of Electrically Programmable Memory Cells," discloses an apparatus directed to verifying the state of a plurality of electrically programmable memory cells.


U.S. Patent 5,444,656 to Bauer et al., "Apparatus for Fast Internal Reference Cell Trimming," discusses a method to trim reference cells, especially for memories with multi bits per cell.

U.S. Patent 6,075,727 to Morton et al., "Method and Apparatus for Writing an Erasable Non-Volatile Memory," discloses a method for writing to a bit of a non-volatile memory by alternately applying programming and erase voltages to a control gate wordline of a memory cell.

U.S. 6,031,760 to Sakui et al., "Semiconductor Memory Device and Method of Programming the Same," discloses an electrically programmable nonvolatile semiconductor memory device, a method of programming the memory, and method of verify reading after programming operation of the memory device.

U.S. Patent 6,009,015 to Sugiyama, "Program-Verify Circuit and Program-Verify Method," discusses a program-verify circuit for an electrically re-writable memory cell.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449



INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Doc No. (Optional)	Application Number
HA10-02-005	10/699,331
Applicant	
Ki-Tae Park et al.	
Filing Date	Group Art Unit
10/31/03	

U. S. PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
6618297	9/9/03	Manea	365	189.09	8/2/02
6044019	3/28/00	Cernea et al.	365	185.21	10/23/98
5712815	1/27/98	Bill et al.	365	185.03	4/22/96
5124945	6/23/92	Schreck	365	185	7/29/91
5444656	8/22/95	Bauer et al.	365	189.01	6/2/94
6075727	6/13/00	Morton et al.	365	185.22	7/29/98
6031760	2/29/00	Sakui et al.	365	185.21	7/29/98
6009015	12/28/99	Sugiyama	365	185.22	5/4/99

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
					YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Portion of Pages, Etc.)

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.